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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/895,524	06/28/2001	Rafael A. Mena	TI-29612	8193

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EXAMINER
FOONG, SUK SAN

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 12/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/895,524	MENA ET AL.
	Examiner	Art Unit
	Suk-San Foong	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) 13-18 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claims 1-12, in Paper No. 4 is acknowledged.

Claim Rejections - 35 USC § 112

2. Claims 1-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 2, it is questioned what is recited through the use of "on the order of".

4. Claims 5 and 6, it unclear what is recited through the term "approximately".

5. In claim 1, line 6, it is questioned what is recited through the use of "closely-spaced".

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 1, 3, 5, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in combination with Jang et al. ('808).

AAPA discloses a prior art method of forming interconnects in integrated circuit devices which includes forming liner 14 over a semiconductor body 10 with metal leads 12 (Instant p. 1, lines 23-25, and Fig. 1), subsequently forming gap-fill 16 layer such as HSQ over liner 14, (Instant p. 1, lines 25-26), then forming dielectric layer 18 such as PETEOS over gap-fill layer 16 (Instant p. 1, lines 26-27), and subsequently forming via to metal leads 12 (Instant p. 1, line 28 to Instant p. 2, line 8).

AAPA does not disclose forming liner layer through HDP (high density plasma) with a portion of the liner layer over metal leads having sloped edges.

Jang et al. discloses a method of forming inter-level metal dielectric layer in microelectronics fabrication which includes providing forming conductive leads 12a and 12 b over substrate 10 (Col. 5, lines 13-20, and 36-39, and Fig. 1), then forming HDP liner layer 14 comprised of silicon oxide over substrate 10 and conductive leads 12a and 12b where a portion

of HDP liner layer 14 has sloped edges and triangular in shape (Col. 5, lines 53-56, and Col. 6, lines 3-8), then forming gap-filling layer 18 over HDP liner layer 14 (Col. 6, lines 41-44, and Fig. 3), and subsequently forming dielectric layer 29 comprised of PETEOS over gap-filling layer 18 (Col. 7, lines 3-8, and Fig. 4).

It would have been within the scope to one ordinary skill in the art to combine both teachings because it would enable formation of liner 14 of AAPA to be performed and obtain further advantage of improving the thickness profile of liner layer over the topography of the conductive leads (Jang et al., Col. 6, lines 3-8).

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Jang et al. ('808) as applied to claims 1, 3, 5 and 12 above.

The combination process does not disclose that the sloped edges have a slope on the order of 45°.

The choice of thickness of gate electrode material would have been a matter of routine optimization to achieve the desired device density on the finished wafer and the desired device characteristics of the device to be formed. (See MPEP 2144.05)

10. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Jang et al. ('808) as applied to claims 1, 3, 5 and 12 above, and further in view of Shields ('850).

The combination process does not disclose that the dielectric layer is comprised of silane based oxide.

The combination process does not disclose that the gap-fill layer is comprised of spin-on glass.

Shields discloses a method of forming an interconnection pattern for semiconductor devices which includes providing metal leads 21A and 21B over substrate 20 (Col. 4, lines 20-24, and Fig. 2), subsequently forming gap-fill layer 23 comprised of materials such as spin-on glass (SOG) or HSQ over metal leads 21A and 21B and filling the gaps in between (Col. 4, lines 32-32), and then applying dielectric layer 24 such as silicon oxide derived from TEOS or silane by PECVD.

It would have been within the scope to one ordinary skill in the art to combine both teachings because it would enable formation of dielectric layer 18 of AAPA to be performed.

It would have been within the scope to one ordinary skill in the art to combine both teachings because it would enable formation of gap-fill layer 16 of AAPA to be performed.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Jang et al. ('808) as applied to claims 1, 3, 5 and 12 above, and further in view of Bothra et al. ('102).

The combination process does not disclose the step recited in claim 6.

Bothra et al. discloses a method of forming semiconductor devices with metallization lines which includes forming liner layer 116 over metallization line 112 formed on semiconductor substrate 110 through HDPCVD deposition where a portion of liner layer 116 over metallization line 112 has sloped edges and trapezoidal in shape (Col. 8, lines 5-24, and Fig. 3B), subsequently depositing dielectric layer 118 over liner layer 116 and substrate 110 (Col. 8,

lines 49-51, and Fig. 3C), and then forming via through dielectric layer 118 to metallization line 112 (Col. 8, lines 59-62, and Fig. 3D).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Bothra et al. with the combination process because it would enable formation of liner layer 14 of AAPA to be performed.

12. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Jang et al. ('808) as applied to claims 1, 3, 5 and 12 above.

The combination process does not disclose the step recited in claim 7.

The choice of etch-to-deposition ratio in forming HDP liner layer would have been a matter of routine optimization to achieve the desired profile given the width and spacing of the metal lines; in view of the disclosure of Kelkar ('367, see Abstract). (See MPEP 2144.05)

13. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Jang et al. ('808) as applied to claims 1, 3, 5 and 12 above, and further in view of Aug et al. ('644).

The combination process does not disclose that the HDP liner layer is comprised of undoped silicon dioxide.

Aug et al. discloses forming a liner layer 14 comprised of undoped silicon dioxide such as USG (undoped silicate glass) over metal structure 12 (Col. 3, lines 28-30, and Fig. 1), and then forming gap-fill layer 16 over liner layer 14 (Fig. 2).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Aug et al. with the combination process because it would enable formation of liner layer 14 of the combination process to be performed.

14. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Jang et al. ('808) as applied to claims 1, 3, 5 and 12 above, and further in view of Tsai et al. ('394).

The combination process does not disclose that the HDP liner layer is comprised of fluorinated HDP oxide.

Tsai et al. discloses a method of forming multi-level interconnects which includes depositing liner layer 204 comprised of fluorinated oxide such as fluorinated silicon glass (FSG) through HDPCVD over metal leads 202 formed on substrate 200 (Col. 3, lines 10-24), and subsequently depositing gap-fill layer 206 over liner layer 204 thereby filling gaps between metal leads 202 (Col. 3, lines 25-29, and Fig. 2A).

It would have been within the scope to one ordinary skill in the art to combine the teachings of Tsai et al. with the combination process because it would enable formation of liner 14 of the combination process to be performed.

15. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in combination with Jang et al. ('808) as applied to claims 1, 3, 5 and 12 above, and further in view of Wolf.

The combination process does not disclose that the HDP liner layer is comprised of phosphorus HDP oxide.

Wolf discloses forming doped silicon dioxide film such as phosphorus doped TEOS as a poly-metal interlevel dielectric material (PMD) in a multilevel-interconnect process (p. 194).

It would have been within the scope to one ordinary skill in the art the combine the teachings of Wolf with the combination process because it would enable formation of liner layer 14 of the combination process to be performed.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suk-San Foong whose telephone number is 703-305-0383. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 (7724, 3431, 3432).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

GF
December 16, 2002

George Fourson
Primary Examiner
Art Unit 2823